

FRANCISCO E. ALDERETE

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TARGETED OBJECTIVE: Senior Hardware Verification Engineer specializing in UVM/SystemVerilog methodologies and the verification of complex Ethernet subsystems. Track record of building scalable, reusable verification environments, and driving designs to successful tapeout within aggressive schedules. Deep expertise in object-oriented testbench architecture, rapid testcase development, and systematic debug across MAC/PCS/SerDes and high-speed datapaths. Collaborative partner to RTL, firmware, and architecture teams, with strong communication skills and a reputation for turning ambiguous requirements into executable verification strategies.

WORK EXPERIENCE:

Intel Corporation: Hardware Design Verification Engineer

Aug 2022 -
Present

- Performed **pre-silicon verification** of Ethernet MAC/PCS and subsystem datapaths aligned with IEEE 802.3 and related protocol specifications.
- Built and maintained **UVM/SystemVerilog** environments to automate sub system bringup which enabled faster validation for other sub system features as basic functionality was automated for different datarates/protocols.
- Led **testcase bring-up**, debug, and regression enablement for complex SoC-level integrations.
- Implemented **error injection** using BFM's to validate DUT robustness (link down, interrupts, malformed frames, recovery scenarios) and to satisfy compliance requirements.
- Authored and executed **comprehensive test plans** covering datapath validation, frame stability, error handling, and timing checks across the subsystem.
- Drove **latency validation** for critical datapath components by correlating architectural expectations with measured simulation results; contributed to sign-off criteria for tapeout.
- Verified and programmed **latency registers** with configurable tolerances to ensure operation within defined timing margins.
- Developed **Python and Bash** automation to accelerate regression analysis, waveform triage, and reporting.
- Leveraged internal **AI-based tooling** to improve productivity in scripting, data parsing, and simulation result analysis.
- Collaborated within large teams using **Git-based workflows** (GATEKEEPER)
- Experienced with industry-standard simulators including **Synopsys VCS**, Cadence, and Mentor Graphics tools.
- Served as **documentation owner** bridging RTL and validation teams; produced clear internal and customer-facing subsystem specifications.

Raytheon: Hardware Design Verification Engineer

Apr 2019 -
Jul 2022

- Performed **pre-silicon netlist and DFT verification** including scan chain, MBIST, fuse, and **JTAG (IEEE 1149.1)** validation, contributing to successful ASIC **tapeout**.
- Executed **ECO flows** with synthesis and validated updates through **Logic Equivalence Checking (LEC)** to maintain sign-off confidence.
- Built reusable **OOP UVM/SystemVerilog** environments
- Developed automation and build infrastructure using **Perl, Python, Bash/Csh, Tcl, and GNU Make**, accelerating debug and tapeout readiness.
- Partnered with DFT, RTL, and backend teams to resolve integration issues and drive the program to **tapeout**.

Honeywell FM&T: Electrical Engineer

Oct 2017 -
Mar 2019

- Process Development used by technicians to build complex electrical systems

EDUCATION:

The University of Texas at Dallas

- Bachelors of Science in Electrical Engineering